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L8 same (core adj1 device)	2

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L1: Entry 2 of 2 File: USPT Jan 3, 2006

DOCUMENT-IDENTIFIER: US 6983405 B1
TITLE: Method and apparatus for testing circuitry embedded within a field programmable gate array

Brief Summary Text (6):
FIG. 1 illustrates a generic schematic block diagram of an FPGA 110. The FPGA 110 includes configurable logic fabric 112 (containing programmable logic gates and programmable interconnects) and configurable input/output blocks 114. The configurable input/output blocks 114 are fabricated on the perimeter of a substrate supporting the FPGA 110 and coupling to the pins of the integrated circuit to allow access to the configurable logic fabric 112.

Brief Summary Text (7):
The logic fabric 112 may be configured to perform a wide variety of functions corresponding to particular end user applications. For example, the configurable logic fabric 112 may be configured in a symmetric array arrangement, a row-based arrangement, a column based arrangement, a hierarchical programmable logic device arrangement, or a sea-of-gates arrangement, each having different functional advantages.

Brief Summary Text (11):
FIG. 3 illustrates a schematic block diagram of the configurable logic fabric 112 being implemented in a row-based arrangement. In this configuration, the logic fabric 112 includes a plurality of logic blocks 216 arranged in rows. Between each row of the logic blocks are programmable interconnections 218. Programmable interconnections 218 may be implemented utilizing static RAMs, dynamic RAMS and NVRAM, EPROM technology, and/or EEPROM technology.

Brief Summary Text (13):
FIG. 5 illustrates the configurable logic fabric 112 being implemented as a hierarchical logic device. In this implementation, the configurable logic fabric 112 includes logic device blocks 522 and programmable interconnections 218. As shown, four logic device blocks 522 are in the corners with an interconnect 218 in the middle of the logic device blocks. In addition, the interconnects include lines coupling the configurable logic device blocks 522 to the interconnect 218. As such, the logic device blocks 522 may be configured to operate singularly or in combination with other logic blocks 522 according to the programming of the programmable interconnections 218.

Brief Summary Text (16):
To mitigate some of the disadvantages of FPGAs with respect to ASICs, some FPGA manufacturers are including ASIC-like functions on the same substrate as the configurable logic fabric. For example, FPGAs are now commercially available that include RAM blocks and/or multipliers in the configurable logic fabric 112. As such, the logic fabric 112 does not have to be configured to perform RAM functions and/or multiplier functions when such functions are needed. Thus, for these functions, significantly less die area is needed within the FPGA.

Description Paragraph (4):
FIG. 2 illustrates a schematic block diagram of the configurable logic fabric of the programmable gate array of FIG. 1 configured in a symmetrical array;

Description Paragraph (37):
Generally, the present invention provides interconnecting logic that interfaces an embedded fixed logic circuit, or circuits, with configurable logic fabric of a field programmable gate array. The interconnecting logic enables any fixed logic circuit (e.g., a digital signal processor, microprocessor, physical layer interface, link layer interface, network layer interface, audio processor, video graphics processor, and/or applications-specific integrated circuit) to be embedded within the configurable logic fabric of a field programmable gate array. In addition, the interconnecting logic provides connectivity between the fixed logic circuit and the configurable logic fabric such that the fixed logic circuit functions are an extension of the configurable logic fabric.

Description Paragraph (38):
The interconnecting logic includes interconnecting tiles and may further include interfacing logic. The interconnecting tiles provide selective connectivity between inputs and/or outputs of the fixed logic circuit and the interconnects or programmable interconnections of the configurable logic fabric. The interfacing logic, when activated to be electrically present, provides logic circuitry that conditions data transfers between the fixed logic circuit and the configurable logic fabric. The conditioning of the data may be format changes, parallel-to-serial conversion, serial-to-parallel conversion, multiplexing, de-multiplexing, performing Boolean logic functions, etc. With such interconnecting logic, any fixed logic circuit may be readily embedded within a programmable gate array to provide additional functionality to the end users of FPGAs.

Description Paragraph (39):
The present invention can be more fully described with reference to FIGS. 6 through 33. FIG. 6 illustrates a block diagram of a field programmable gate array 300. The field programmable gate array 300 includes the configurable logic fabric 112, the configurable input/output blocks 114, a fixed logic circuit 632 and interconnecting logic 634. The fixed logic circuit 632 may be a digital signal processor, microprocessor, physical layer interface, link layer interface, network layer interface, audio processor, video graphics processor, logic circuitry, and/or applications-specific integrated circuits.

Description Paragraph (40):
Typically, the fixed logic circuit 632 includes a plurality of inputs and a plurality of outputs, which are represented by input/output ports 636, 638, 640 and 642. The input/output ports 636 642 are operably coupled to the interconnecting logic 634, which provides connectivity between the input/output ports of the fixed logic circuit 632 with the configurable logic fabric 112 of the FPGA 300. It should be noted that more than one fixed logic circuit can be included in the programmable gate array.

Description Paragraph (41):
The configurable logic fabric 112 includes a plurality of configurable logic blocks (CLBs) and programmable interconnects. The architecture of the configurable logic fabric may be row or column based, hierarchical-PLD, symmetrical array, and/or a sea-of-gates. The configurable logic blocks, interconnects, and I/O blocks may be, for example, of the type manufactured and distributed by Xilinx, Inc. The interconnects may include a plurality of switch matrix devices that utilize static RAM cell technology, anti-fuse cell technology, EPROM transistor technology, and/or EEPROM transistor technology.

Description Paragraph (42):
The field programmable gate array 300 may be implemented as an integrated circuit

wherein the configurable I/O blocks 114, configurable logic fabric 112, the interconnecting logic 634 and the fixed logic circuit 632 are fabricated on a substrate. In one embodiment, the circuitry of each of these elements 112, 114, 632 and 634, are implemented using CMOS technology on a silicon substrate. However, as one of average skill in the art will appreciate, other integrated circuit technologies and substrate compositions may be used.

Description Paragraph (43):
In operation, the interconnecting logic 634 provides coupling between the configurable logic fabric 112 and the fixed logic circuit 632. As such, end users of the field programmable gate array 300 may program it by treating it as a component of the configurable logic fabric 112. For example, if the fixed logic circuit 632 includes a microprocessor, the interconnecting logic 634 may include memory for storing programming instructions and data in addition to connectivity to memory of the FPGA 300.

Description Paragraph (44):
Accordingly, the configurable logic fabric 112 is configured to perform desired functions in combination with the fixed logic functions of the microprocessor. Thus, with an embedded microprocessor, the field programmable gate array 300 offers the flexibility of an FPGA, with the processing efficiency of an application-specific integrated circuit microprocessor. In addition, by embedding a microprocessor within the configurable logic fabric 112, as opposed to having two separate integrated circuits (one for the microprocessor and another for the FPGA), power consumption is reduced due to the elimination of interconnecting pins and traces between the two separate integrated circuits. Further, the field programmable gate array 300 requires less printed circuit board real estate than separate integrated circuits for an FPGA and a microprocessor.

Description Paragraph (45):
FIG. 7 illustrates a graphical diagram of an alternate field programmable gate array 500. The field programmable gate array 500 includes the configurable logic fabric 112, the configurable input/output blocks 114, a 1.sup.st fixed logic circuit 632, 1.sup.st interconnecting logic 634, a 2.sup.nd fixed logic circuit 752 and 2.sup.nd interconnecting logic 754. In this illustration, the 1.sup.st interconnecting logic 634 and 1.sup.st fixed logic circuit 632 are as generally described with reference to FIG. 6.

Description Paragraph (46):
The 2.sup.nd fixed logic circuit 752 may include any logic functions, including those of a digital signal processor, microprocessor, physical layer interface, link layer interface, network layer interface, audio processor, video graphics processor, logic circuitry, and/or an application-specific integrated circuit. The 2.sup.nd fixed logic circuit 752 includes a plurality of input/output ports 756, 758, 760 and 762 that allow it to interface with the 2.sup.nd interconnecting logic 754. The 2.sup.nd interconnecting logic 754 provides the connectivity between the 2.sup.nd fixed logic circuit 752 and the configurable logic fabric 112.

Description Paragraph (47):
FIG. 8 illustrates a graphical diagram of another field programmable gate array 700. The field programmable gate array 700 includes the configurable logic fabric 112, the configurable input/output blocks 114, and four fixed logic circuits 632, 752, 872 and 876. The structure of each fixed logic circuit is similar to the fixed logic circuit shown in FIG. 7 (note that the I/Os in each fixed logic circuit are not shown because of the limited size of the drawings). Each fixed logic circuit 632, 752, 872 and 876 has its own corresponding interconnecting logic 634, 754, 874 and 878, respectively. The interconnecting logic 634, 754, 874 and 878 provide its respective fixed logic circuit connectivity to the configurable logic fabric 112.

Description Paragraph (49):

FIG. 9 illustrates a more detailed graphical diagram of a portion of the field programmable gate array 300 with an embedded device of FIG. 6. While FIG. 9 is illustrated with reference to the FPGA 300 of FIG. 6, the concepts regarding the interconnecting logic 634 is equally applicable to the interconnecting logic 754 of FIG. 7, and the interconnecting logic 754, 874, and 878 of FIG. 8. As one of average skill in the art will appreciate, any number of fixed logic circuits may be embedded within the configurable logic fabric using interconnecting logic.

Description Paragraph (50):
As shown in FIG. 9, the configurable logic fabric 112 includes a plurality of configurable logic blocks (CLBs) 980, a plurality of block random access memory (RAM) 990, and a plurality of multipliers 992. The configurable I/O block section 114 shown on FIG. 1 includes a plurality of individual I/O blocks (10B) 986 and a plurality of digital clock managers (DCM) 984. The operations of the configurable logic blocks 980, the digital clock managers 984, the input/output blocks 986, the block RAM 990, and the multipliers 992 function in a similar manner as corresponding components found in the family of field programmable gate arrays designed and manufactured by Xilinx, Inc.

Description Paragraph (66):
FIGS. 15, 16 and 17 are functional schematic diagrams illustrating a plurality of arrangements of a fixed logic device formed or "cut into" a configurable logic fabric in which the embedded device includes interconnecting logic between it and the configurable logic fabric according to various embodiments of the present invention. As may be seen in FIG. 15, a high speed data interface 1532 is surrounded by a 1.sup.st interconnecting logic 1536 while a fixed logic processing module 1534 is surrounded by a 2.sup.nd interconnecting logic 1538. FIG. 16 is similar to FIG. 15 with the exception that the high-speed data interface 1632 is placed at the edge of the configurable logic fabric. Accordingly, the 1.sup.st interconnecting logic 1636 is only formed to surround the high-speed data interface 1632 on those sides that are bound by the configurable logic fabric. FIG. 17 is similar to FIG. 16 with the exception that the high-speed data interface is placed within a corner of the configurable logic fabric 112. Accordingly, the 1.sup.st interconnecting logic 1736 is formed on only two sides of the high-speed data interface 1732.

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L5: Entry 1 of 2 File: USPT Feb 7, 2006

DOCUMENT-IDENTIFIER: US 6996758 B1
TITLE: Apparatus for testing an interconnecting logic fabric

Abstract Text (1):
A circuit that includes a core device that is embedded within fixed interfacing logic circuitry that, in turn, is embedded in an FPGA fabric. The FPGA fabric may be configured into a test mode of operation to test either the embedded device or fixed logic devices formed within the fixed interfacing logic. While the FPGA is configured in a test mode, test circuitry and communication paths are made present within the fixed interfacing logic circuitry to facilitate the testing. Additionally, the test circuitry comprises isolation circuitry that is formed between various modules and circuits that are to be tested to isolate the device under test and to produce test signals thereto and there from during testing operations.

Brief Summary Text (24):
The test circuitry within the gasket further includes isolation circuit elements that allow the FPGA fabric (as configured for testing) to have direct access to the input/output of the device under test whether it is the fixed logic device formed within the gasket or an embedded core processor. An FPGA fabric that is configured for testing can perform structural tests for a specific device because the necessary access to the device inputs and outputs are provided, at least in part, by test circuitry formed within the gasket. Because test vectors or signals may be provided to the embedded device(s) as well as the fixed logic circuitry, structural testing of the entire FPGA is supported thereby enabling a tester to determine with a large degree of certainty whether the FPGA is operational.

Description Paragraph (49):
FIG. 9 illustrates a more detailed graphical diagram of a portion of the field programmable gate array 300 with an embedded device of FIG. 6. While FIG. 9 is illustrated with reference to the FPGA 300 of FIG. 6, the concepts regarding the interconnecting logic 634 is equally applicable to the interconnecting logic 754 of FIG. 7, and the interconnecting logic 754, 874, and 878 of FIG. 8. As one of average skill in the art will appreciate, any number of fixed logic circuits may be embedded within the configurable logic fabric using interconnecting logic.

Description Paragraph (61):
FIG. 13 is a flow chart illustrating a method for testing fixed logic circuitry within the interfacing logic according to one embodiment of the present invention. Generally the method includes configuring the FPGA into a test mode (step 1304). Thereafter, test signals are transmitted to a test multiplexer within the interfacing logic (step 1308). The test signals are then transmitted from the test multiplexer to fixed logic circuitry (either an embedded device or fixed logic formed within the gasket or interfacing circuitry (step 1312). The test signal outputs from the fixed logic circuitry are then transmitted through a communication path formed within the gasket (interfacing logic) to the FPGA fabric (step 1316). In one embodiment of the invention, the FPGA fabric is configured to analyze the test signal outputs to determine whether the embedded core device passed or failed the test. In another embodiment of the invention, the test signal outputs are merely conducted through the FPGA fabric to an external device, or system, such as

a tester, to determine pass or fail.

Description Paragraph (72):
During testing of the fixed logic core processor 2016 (an embedded device; for example, a Power PC), the FPGA fabric 2000 is configured to access, stimulate, and receive outputs from the fixed logic core processor 2016. Likewise, during testing of the gasket logic 2020, the FPGA fabric 2000 is configured to access, stimulate, and receive output from the gasket logic 2020.

Description Paragraph (110):
FIG. 29 is a functional block diagram illustrating the use of a scan chain in an FPGA fabric to test an embedded device according to one aspect of the present invention. As mentioned before, a plurality of test configurations may be defined, each of which is for performing a specified test. Thus, one particular scan chain is for establishing logic states and circuit configuration within the FPGA fabric to support testing of the embedded device, as shown in the functional block diagram of FIG. 29.

Description Paragraph (122):
FIG. 31 is a flow chart illustrating a method for testing an embedded core device according to one embodiment of the present invention. As has been described before, the FPGA disclosed herein includes an embedded cored device that is surrounded by interfacing logic that is for interfacing the embedded cored device to the FPGA fabric, among other purposes. A first step in testing such an embedded core device, therefore, is to configure the FPGA into a mode for performing the testing of the embedded core device (step 3104). As a part of configuring the FPGA for the embedded core test, communication paths in the interfacing logic must be created or made electrically present (step 3108). These communication paths are useful for producing scan chains, if necessary, to the embedded core device, as well as for producing test data. Thus, the next step includes producing test vectors within the scan chains to the embedded core device (step 3112). Additionally, the inventive process includes producing test data and conducting the test data through the interfacing logic to the inputs of the core device (step 3116). Once the test has been set up through the scan chains and through the data being produced to the device under test, a clock pulse is generated to prompt the embedded device to process the data and produce resulting outputs. Accordingly, the invention includes, after generating the clock pulse, receiving output scan chains, or at least one output scan chain, from the embedded core device (step 3120). The output scan chains are then conducted to an external tester (step 3124) where it may determine whether electrical integrity or functional integrity exists (step 3128).

CLAIMS:

14. A method for testing an FPGA, comprising: configuring the FPGA for test and forming a scan chain internal to the FPGA to test a fixed logic embedded device within the FPGA; configuring a multiplexer to receive and forward an output test signal; transmitting the output test signal from the fixed logic embedded device to a multiplexer formed within a gasket; and transmitting the output test signal from the multiplexer to an FPGA fabric portion.

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L5: Entry 2 of 2 File: USPT Jan 3, 2006

DOCUMENT-IDENTIFIER: US 6983405 B1
TITLE: Method and apparatus for testing circuitry embedded within a field programmable gate array

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A circuit that includes a core device that is embedded within fixed interfacing logic circuitry that, in turn, is embedded in an FPGA fabric. The FPGA fabric may be configured into a test mode of operation to test either the embedded device or fixed logic devices formed within the fixed interfacing logic. While the FPGA is configured in a test mode, test circuitry and communication paths are made present within the fixed interfacing logic circuitry to facilitate the testing. Additionally, the test circuitry comprises isolation circuitry that is formed between various modules and circuits that are to be tested to isolate the device under test and to produce test signals thereto and therefrom during testing operations.

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